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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,193	08/30/2006	**Mohamed Azimane**	US04 0145 US3	5900

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EXAMINER	
MCMAHON, DANIEL F	

ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/591,193	AZIMANE ET AL.	
	Examiner	Art Unit	
	DANIEL F. MCMAHON	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/22/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 24 are presented for examination.

Priority

1. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) is acknowledged.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on August 30, 2006 was received. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. The application appears to be International form, standard US format is required (37 C.F.R. 1.77)

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

4. The specification is objected to for failure to provide a background of the invention. The specification fails to distinguish applicant's invention from what is old (37 C.F.R. 1.71(b)).

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. The specification is objected to for failure to comply with 35 U.S.C. 112, first paragraph, which, requires the specification to be written in "full, clear, concise, and exact terms." The language in the specification "sprit … of the invention" (Page 4, line 5; Page 7, line 11) is not clear and concise in regard to the subject matter claimed.

The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph.

Claim Objections

7. Claim 9 is objected to because of the following informalities: "the control circuitry for receiving" lacks proper antecedent basis in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Regarding claim 9, "and for providing an internal clock signal in dependence thereupon to the internal memory block" is vague. It is unclear how "providing" is dependant on the internal memory block or alternatively what is referenced by "thereupon".

9. Regarding claim 17, "for providing at least an internal clock signal in dependence thereupon to the at least an internal memory block" is vague. It is unclear how "providing" is dependant on the internal memory block, or alternatively what is referenced by "thereupon".

Prior Art Rejections

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4 – 13, 16 – 20, 23, and 24 are rejected under 35 U.S.C. 102(b) as being anticipate by Churchill et al. U.S. Patent 6,115,836 (herein Churchill).

10. Regarding claim 1, Churchill discloses: A method for providing an external clock signal (figure 2, clk) to an internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218) of a self-timed memory (figure 2, element 200) comprising: receiving an

internal clock signal (figure 9, element 916) from a clock monitor of the self-timed memory (figure 9, element 902; figure 11c, element 1102); receiving an external clock signal (figure 2, clk); receiving a control signal (figure 9, element 912); and, providing, in dependence upon the control signal, the internal clock signal to the internal memory block during a normal mode of operation of the self-timed memory (column 18, lines 6 – 12), and the external clock signal to the internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10).

11. Regarding claim 2, Churchill additionally discloses: the external clock signal received during test mode is generated according to a predetermined test pattern (column 18, lines 46 – 48; column 19, lines 5 – 10)

12. Regarding claim 4, Churchill additionally discloses: the external clock signal received during test mode comprises a duty cycle higher than a 50% duty cycle of the internal memory block (column 18, lines 46 – 48; column 19, lines 5 – 10)

13. Regarding claim 5, Churchill additionally discloses: internal clock signal is provided to the internal memory block in absence of a control signal (column 19, lines 5 – 10).

14. Regarding claim 6, Churchill additionally discloses: a control signal indicating initiation of the test mode is provided (column 19, lines 5 – 10).

15. Regarding claim 7, Churchill additionally discloses: a control signal indicating termination of the test mode is provided (column 19, lines 5 – 10).

16. Regarding claim 8, Churchill additionally discloses: at least a control signal is provided during the test mode (column 19, lines 5 – 10).

17. Regarding claim 9, Churchill discloses: A self-timed memory (figure 2) comprising: an internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218), a clock monitor (figure 9, 902) for receiving an external clock signal (figure 2, clk) and for providing an internal clock signal (figure 9, element 902) in dependence thereupon to the internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a test system (figure 9, element 908, 910) interposed between the clock monitor (figure 9, 902) and the internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218). The test system comprising: an internal clock signal input port (figure 9, element 908) in signal communication with the clock monitor for receiving the internal clock signal (figure 9, element 916); an external clock signal input port (figure 9, element 910) for receiving the external clock signal (figure 9, element 914); a control signal input port (figure 9, element 908) for receiving a control signal (figure 9, element 912); an output port in signal communication with the internal memory block (figure 2, element 222); and, a multiplexer in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input port and the output port (figure 9, element 908, 910); the control circuitry for receiving the internal clock signal,

the external clock signal, and the control signal, and for providing, in dependence upon the control signal, the internal clock signal via the output port to the internal memory block during a normal mode of operation of the self-timed memory (column 18, lines 6 – 12), and for providing the external clock signal to the internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10).

18. Regarding claim 10, Churchill additionally discloses: the clock monitor comprises an input port for receiving the external clock signal (figure 9, element 902, signal 914) and wherein the input port is connected to the external clock signal input port of the test system (figure 9, element 908. 910, signal 914).

19. Regarding claim 11, Churchill additionally discloses: test circuitry in signal communication with the test system (figure 2, element 212), the test circuitry for providing a control signal to the test system and for providing the external clock signal to the test system during test mode (column 5, lines 13 – 25).

20. Regarding claim 12, Churchill additionally discloses: the internal memory block comprises an address decoder (figure 2, element 204, 208).

21. Regarding claim 13, Churchill additionally discloses: the internal memory block comprises a sense amplifier (figure 2, element 214).

22. Regarding claim 16, Churchill additionally discloses: the internal memory block comprises input/output latches (figure 2, element 216, 218).

23. Regarding claim 17, Churchill discloses: A self-timed memory (figure 2) comprising: at least an internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a clock monitor (figure 9, 902) for receiving an external clock signal (figure 2, clk) and for providing at least an internal clock signal (figure 9, element 902) in dependence thereupon to the at least an internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a test system (figure 9, element 908, 910) interposed between the clock monitor (figure 9, 902) and the at least an internal memory block(figure 2, element 202, 204, 206, 208, 214, 216, 218). The test system comprising: at least an internal clock signal input port (figure 9, element 908) in signal communication with the clock monitor for receiving at least an internal clock signal (figure 9, element 916); an external clock signal input port (figure 9, element 910) for receiving the external clock signal (figure 9, element 914); a control signal input port (figure 9, element 908) for receiving a control signal (figure 9, element 912); at least an output port in signal communication with the at least an internal memory block (figure 2, element 222); and, control circuitry in signal communication with the at least an internal clock signal input port, the external clock signal input port, the control signal input port and the at least an output port (figure 9, element 908, 910); the control circuitry for receiving the at least an internal clock signal, the external clock signal, and the control signal, and for providing, in dependence upon the control signal, the at least an internal

clock signal via the at least an output port to the at least an internal memory block during a normal mode of operation of the self-timed memory (column 18, lines 6 – 12), and for providing the external clock signal to at least one of the at least an internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10).

24. Regarding claim 18, Churchill additionally discloses: the control circuitry comprises a multiplexer (figure 9, element 908, 910).

25. Regarding claim 19, Churchill additionally discloses: the at least an internal memory block comprises an address decoder (figure 2, element 204, 208).

26. Regarding claim 20, Churchill additionally discloses: the at least an internal memory block comprises a sense amplifier (figure 2, element 214).

27. Regarding claim 23, Churchill additionally discloses: the at least an internal memory block comprises input/output latches (figure 2, element 216, 218).

28. Regarding claim 24, Churchill additionally discloses: test circuitry in signal communication with the test system (figure 2, element 212), the test circuitry for providing a control signal to the test system and for providing the external clock signal to the test system during test mode (column 5, lines 13 – 25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. U.S. Patent 6,115,836 (herein Churchill).

29. Regarding claim 3, Churchill teaches the limitations of the parent claim, claim 2. Churchill additionally teaches: the delay circuit programmed for generating an internal clock with a duty cycle less then 50% (column 17, lines 33 – 50). Churchill additionally teaches: an external clock with a configurable duty cycle (column 19, lines 5 – 10).

Churchill does not explicitly teach: the external clock signal received during test mode comprising a duty cycle lower than a 50% duty cycle of the internal memory block.

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, an internal clock signal with a duty cycle less then 50%, with the teaching of an external clock signal with a configurable duty cycle, for the purpose of creating an external clock signal with a duty cycle of less then 50%. An external clock signal with a configurable duty cycle is a well known device in the art. A clock signal with duty cycle of less then 50% is a well known technique in the art. One of ordinary skill in the art, at the time of the invention, would have recognized

that applying the known technique to the known device would have yielded predictable results.

Claims 14, 15, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill, in view of Chol, U.S. Patent 6,324,115 (herein Chol).

30. Regarding claim 14, Churchill additionally teaches: the internal memory block comprising a column decoder (figure 2, 208). Churhill does not explicitly teach: the internal memory block comprising a bank decoder.

Chol teaches: an internal memory block comprising a bank decoder (figure 1, element 160).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, and a column decoder, as cited above, with the teaching of Chol, a bank decoder, for the purpose of addressing memory (column 1, lines 19 – 27). A self-timed memory is a well known device in the art. A bank decoder for addressing internal memory blocks is a well known technique. One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable results.

Regarding claim 15, Churchill teaches the limitations of the parent claim, claim 9. Churchill does not explicitly teach: the internal memory block comprising a precharge and discharge circuitry.

Chol teaches: the internal memory block comprising a precharge and discharge circuitry (figure 1, element 310, 320).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, as cited above, with the teaching of Chol, precharge and discharge circuitry. A self-timed memory is a well known device in the art. Precharge and discharge circuitry for accessing internal memory blocks is a well known technique. One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable results.

31. Regarding claim 21, Churchill additionally teaches: the internal memory block comprising a column decoder (figure 2, 208). Churhill does not explicitly teach: the at least an internal memory block comprising a bank decoder.

Chol teaches: an at least an internal memory block comprising a bank decoder (figure 1, element 160).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, and a column decoder, as cited above, with the teaching of

Chol; a bank decoder, for the purpose of addressing memory (column 1, lines 19 – 27). A self-timed memory is a well known device in the art. A bank decoder for addressing internal memory blocks is a well known technique. One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable results.

32. Regarding claim 22, Churchill teaches the limitations of the parent claim, claim 9. Churchill does not explicitly teach: the at least an internal memory block comprising a precharge and discharge circuitry.

Chol teaches: the at least an internal memory block comprising a precharge and discharge circuitry (figure 1, element 310, 320).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an at least an internal memory block, as cited above, with the teaching of Chol; precharge and discharge circuitry. A self-timed memory is a well known device in the art. Precharge and discharge circuitry for accessing internal memory blocks is a well known technique. One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable results.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571)272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

Dfm
08/20/08